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DIALOG(R) File 351:Derwent WPI  
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012770947 \*\*Image available\*\*  
WPI Acc No: 1999-577170/199949

XRPX Acc No: N99-426327

Memory cell of semiconductor memory such as DRAM - has two capacitor connected to drain of transistor whose source and gate are coupled to bit line and word line, respectively

Patent Assignee: FUJITSU LTD (FUIT )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11251534	A	19990917	JP 9846788	A	19980227	199949 B

Priority Applications (No Type Date): JP 9846788 A 19980227

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11251534	A	26	H01L-027/10	

Abstract (Basic): JP 11251534 A

NOVELTY - The gate (G) of the forwarding transistor is connected to the word line (WL). The source (S) is connected to the bit line (BL).

The drain (D) of transistor is connected to the electrodes of one or more capacitors (C1,C2) and forms the semiconductor memory.

DETAILED DESCRIPTION - The capacitor (C1) is a paraelectric capacitor and the capacitor (C2) is ferroelectric capacitor.

USE - In semiconductor memory such as DRAM, FRAM.

ADVANTAGE - Maintains the memory information using the capacitors even when the power supply turns OFF increasing the capability and reliability of semiconductor memory. DESCRIPTION OF DRAWING(S) - The figure shows the circuit diagram of semiconductor memory. (BL) Bit line; (C1,C2) Capacitors; (D) Drain; (G) Gate; (S) Source; (WL) Word line.

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Title Terms: MEMORY; CELL; SEMICONDUCTOR; MEMORY; DRAM; TWO; CAPACITOR; CONNECT; DRAIN; TRANSISTOR; SOURCE; GATE; COUPLE; BIT; LINE; WORD; LINE; RESPECTIVE

Derwent Class: U13; U14

International Patent Class (Main): H01L-027/10

International Patent Class (Additional): G11C-011/22; G11C-014/00; H01L-021/8242; H01L-027/108

File Segment: EPI

Manual Codes (EPI/S-X): U13-C04B1A; U14-A03B4; U14-A03F  
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DIALOG(R) File 345:Inpadoc/Fam.& Legal Stat  
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Basic Patent (No,Kind,Date): JP 11251534 A2 19990917 <No. of Patents:  
001

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Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date
JP 11251534	A2	19990917	JP 9846788	A	19980227

(BASIC)

Priority Data (No,Kind,Date):

JP 9846788 A 19980227

PATENT FAMILY:

JAPAN (JP)

Patent (No,Kind,Date): JP 11251534 A2 19990917

SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURE (English)

Patent Assignee: FUJITSU LTD

Author (Inventor): NAKAMURA SHUNJI

Priority (No,Kind,Date): JP 9846788 A 19980227

Applic (No,Kind,Date): JP 9846788 A 19980227

IPC: \* H01L-027/10; G11C-011/22; G11C-014/00; H01L-027/108;  
H01L-021/8242

Derwent WPI Acc No: \* G 99-577170; G 99-577170

Language of Document: Japanese

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